A LOW-NOISE LOW-POWER SECOND-ORDER COMPENSATED CMOS BANDGAP REFERENCE

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Abstract

The design of a low-noise and low-power second-order bandgap reference voltage source using a linear combination of two base-emitter voltages with only one scaling factor is treated. The design takes into account the temperature dependency of the resistors and the finite current gain of BJT's. The circuit is integrated in a CMOS process. The output voltage is approximately 140 mV with an average temperature dependency of 22.5 ppm/K in the range of 0°C to 120°C. Its equivalent output noise voltage is 57.6*n*V/√Hz. The total current consumption is about 115 μA from a 2V voltage-supply.

Keywords: bandgap reference, negative feedback, systematic design.

1. Introduction

A linear combination of two base-emitter voltages of BJT's, whose collector biasing currents exhibit different temperature dependencies, is sufficient to perform temperature dependency compensation. If one of the scaling factors is chosen to be one then the reference voltage at the output of the bandgap reference becomes technology-determined and has first and second-order frequency temperature.

This paper describes the design of such a bandgap reference circuit with only one scaling factor and optimal noise behaviour. The design is going to be implemented on a CMOS process, therefore the reference BJT's are of the substrate type. The design follows a systematic design approach which is concerned with optimal noise behaviour.

2. The Basic Theory and the Basic Architecture of the Bandgap Reference

Figure 1(a)[10] is a general topology of a second-order bandgap reference. Because a_1 is a constant, if a_1 is shifted after the adder, Figure 1(b), the temperature dependency of the output voltage is unchanged. Thus, a_1 can be removed by setting it as unity as in Figure 1(c). Figure 1(c) shows that now:

$$V_{REF} = V_{BE1} + a_2 V_{BE2} \tag{1}$$

which is a linear combination of two base-emitter voltage. Writing the base-emitter voltage as a Taylor series around a reference temperature T_r[10] results in:

$$V_{BEm}(T) = V_{BEm}(T_r) + \left[V_{BEm}(T_r) - V_G^{'}(0)_m\right]\frac{T-T_r}{T_r} + B_2(\theta_m)\left(\frac{T-T_r}{T_r}\right)^2 + (higher\ order\ terms) \tag{2}$$

where:

$$B_2(\theta_m) = \left[\alpha_2 T_r^2 - \frac{kT_r}{q}(\eta - \theta_m)\frac{1}{2}\right] \tag{3}$$

$$V_G^{'}(0)_m = V_G(T_r) + \alpha_1 T_r - (\eta - \theta_m)\frac{kT_r}{q} \tag{4}$$

in which α_1 and α_2 are the first and the second order Taylor coefficient of the bandgap voltage $V_G(T)$ at T_r, respectively, m is the number of BJT generating the base-emitter voltage, q is the electron charge, k is Boltzmann constant, θ_m is the order of the temperature dependency of BJT_m's biasing current (θ_m =1 means a PTAT current and θ_m = 0 means a constant current), and η is the order of the temperature dependency of the saturation current of the BJTs. Substituting V_{BEm} in Equation (1) with of equation (2) results in[10]:

$$V_{REF} = V_G^{'}(0)_1 + a_2 V_G^{'}(0)_2 \tag{4a}$$

$$a_2 = -\frac{B_2(\theta_1)}{B_2(\theta_2)} \tag{4b}$$

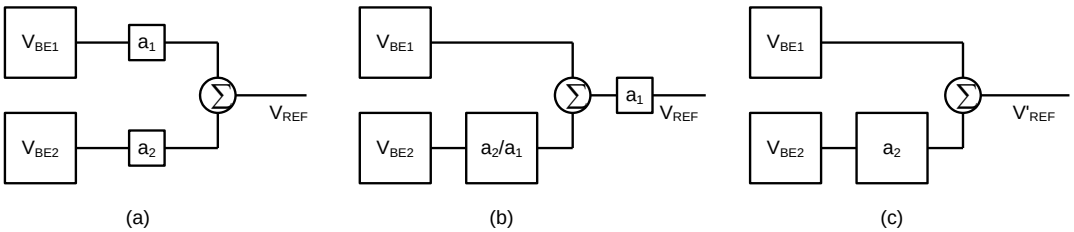

Figure 1. Second-Order Temperature Compensation:
(a) general architecture, (b) shifting a_1 through the adder, (c) a_1 is set to unity.

Thus a_2 is determined by the second order temperature dependency compensation. Thus V_{REF}, which is determined by equation (4a) and (4b), is actually determined by the process selected, represented by η. For AMS CUP (a 0.60 um CMOS technology) η = 5.53. Using Varshini's bandgap energy model[10] and setting θ_1 = 1 and θ_2 = 0, they are obtained: a_2 = –0.87 and V_{REF} = 146.12 mV.

Figure 2 shows the remaining third order temperature dependency of V_{REF}. The mean temperature dependency is approximately 0.6 ppm/K.

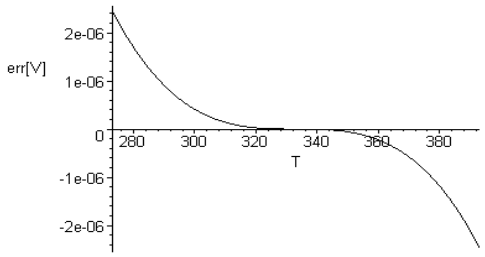

Figure 2. The Remaining 3rd-order Temperature Dependency of V_{REF}.

3. Technology Consideration

There are two process-dependent factors which also influences the temperature dependency of the bandgap reference circuit.

In *AMS CUP* process the available BJT is of PNP type so the biasing current will be more convenient expressed in the emitter current rather than in the collector current. Because the current gain, β, of the BJT available is finite, the emitter current also supplies the base current. This base current gives additional temperature dependency to the base-emitter voltage. The error due to the base-current is expressed as[9]:

$$\Delta V_{BE}(T) = -V_T \ln\left[1+\frac{1}{\beta(T_r)}\cdot\left(\frac{T}{T_r}\right)^{-XTB}\right] \qquad (5)$$

where *XTB* is the order of the temperature dependency of base-current.

Another factor is the resistor used for driving the biasing current experiences also a temperature dependency. This dependency contributes additional temperature dependency to the base-emitter voltage. AMS CUP process only supplies the first order temperature dependency coefficient for its resistor, the error it contributes is[1]:

$$\Delta V_{BE}(T, c_1) = -V_T \cdot \ln\left[1+c_1(T-T_r)\right] \qquad (6)$$

where $V_T = \frac{kT}{q}$.

By expanding Equation (5) and (6) into its Taylor series, the additional first and second order temperature dependency can be found. Adding these additional temperature dependencies into equation (3) and (4a) appropriately will result in a shift in value of a_2, which in return also shifts the value of V_{REF}. The new values after taking these errors into account are: a_2 = –0.88 and V_{REF} = 134.67 mV.

4. Implementation of the Circuit

Figure 1(c) is the basic block of the bandgap reference which is going to be implemented. Its output voltage is expressed in equation (1).

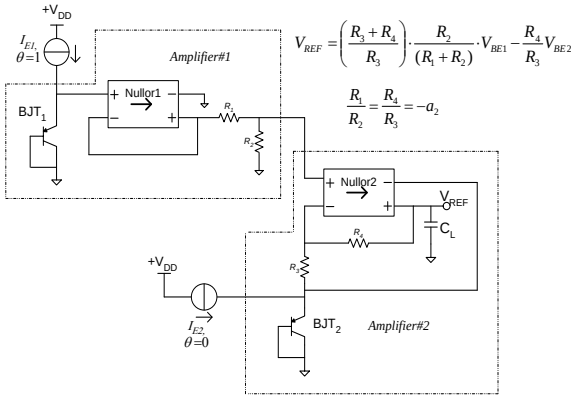

Figure 3. The Bandgap Reference at Nullor Level

4.1 The Basic Circuit Diagram

Figure 3 is the bandgap reference at nullor level which implements Figure 1(c). The output of Figure 3 is expressed as:

$$V_{REF} = \left(\frac{R_3+R_4}{R_3}\right)\cdot\frac{R_2}{(R_1+R_2)}\cdot V_{BE1} - \frac{R_4}{R_3}V_{BE2} \qquad (7)$$

To suit Equation (1) these conditions are required:

$$\frac{R_4}{R_3} = -a_2 \qquad (8)$$

and

$$\frac{R_1}{R_2} = -a_2 \qquad (9)$$

4.2 BJT Biasing

In Figure 3, BJT_1 (BJT_2) is biased at a PTAT (constant) current level.

The minimum noise voltage at the output of the bandgap reference only due to the noise of the reference transistors, equals[10]:

$$\bar{v}_{n,eq} = 10^{-10} V_{REF}\sqrt{\frac{B}{I_{MAX}}} \qquad (10)$$

where $I_{MAX} = I_{C1} + I_{C2}$, the sum of the collector currents of transistor BJT_1 and BJT_2 and B is the bandwidth, chosen 1kHz. Equation (10) then gives approximately I_{MAX} = 5 nA.

Because a_1 = 1 in this design, for optimal noise behavior following condition should be fulfilled[10]:

$$\frac{1}{a_2} = -\frac{I_{C1}}{I_{C2}} \qquad (11)$$

The saturation current of BJT_1 I_{S1} is set equal to of the minimum sized BJT in AMS 0.6 μm CUP process while the saturation current of BJT_2 I_{S2} is set by using N times of the minimum sized BJT, in other words, $I_{S2} = N*I_{S1}$. The relationship of all these parameters and requirements is given as[3]:

$$I_{C2} = I_{S1} \exp\left\{\frac{1}{(1+a_2)}\left[\frac{qV_{REF}}{kT_r} + \ln(-a_2) + a_2 \ln(N)\right]\right\} \quad (12)$$

By plotting I_{C2} as a function of N, a convenient I_{C2} is found when N= 12, which gives these values:

I_{C1} = 6.35 μA and I_{C2}= 5.59 μA.

Consequently I_{MAX}= 11.84 μA, much higher than the minimum current found with Equation (10). Putting I_{C1} and I_{C2} into following equation:

$$I_C(T) = I_S(T)\left[\exp\left(\frac{qV_{BE}}{kT}\right) - 1\right] \quad (13)$$

gives: V_{BE1} = 572.35 mV and V_{BE2} = 497.37 mV.

Because in *CUP* process the available BJT is vertical PNP BJT, biasing current is more convenient to be expressed in its emitter current. For CUP process $\beta(T_r)$ = 17.29, thus:

I_{E1}= 6.71μA and I_{E2}= 5.91μA.

4.3 Developing the Bandgap Reference at Circuit Level

To develop the bandgap reference more systematically the basic circuit in Figure 3 is divided into two amplifiers, i.e.: Amplifier#1, includes BJT_1, Nullor1, R_1 and R_2, and Amplifier#2, includes BJT_2, Nullor1, R_3 and R_4.

The nullors consist of two stages of amplifier in order to achieve relatively high open loop gain. The input stage is a PMOS differential amplifier and the second stage is an NMOS common source amplifier in order to make the circuit operate under a single polarity voltage supply. The restriction in designing the amplifiers is that the current through the resistors must not be higher than its BJT's emitter current.

4.3.1 Amplifier#1

Following the restriction of maximal current through the resistors R_1 and R_2 and fulfilling Equation (9) results in:

R_1 =39.9 $k\Omega$ and R_2 =45.34kΩ.

A convenient level of drain current and the dimension of PMOS for the input stage of the nullor are found by setting such a way that its noise level is a half of it produced by resistors R_1 and R_2. The high-frequency stability of Amplifier#1 is achieved by adding a 2 pF capacitor parallel to R_2 to eliminate the circuit instability at about 9 MHz. Another 2 pF connects the inputs of Nullor1 to keep the voltage at the terminals at the same phase.

4.3.2 Amplifier#2

Doing a similar step as in Section 4.3.1 gives:

R_3 = 32.652 $k\Omega$ and R_4 = 28.733 $k\Omega$.

Because resistors in Amplifier#2 are less than in Amplifier#1, a convenient level of drain current and the dimension of PMOS for the input stage of the nullor are found after following such a way that its noise level equals of it produced by resistors R_3 and R_4. The high-frequency instability is found at 1.8 MHz and eliminated by adding a 5 pF capacitor in series with a 40 $k\Omega$ resistor from the drain of NMOS, the second stage amplifier, to the ground.

4.4 The constant and PTAT current sources

The constant current is required to biasing BJT_2 in Figure 3. In order to make the current generated by the source relatively immune to the disturbance of power source, the voltage to generate the current is fed from the bandgap reference output voltage. Figure 4 shows the nullor-level block diagram of the constant current source which is a transconductance amplifier.

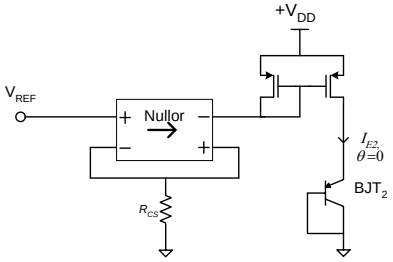

Figure 4. The Constant Current Source and Its Load, BJT_2

For this amplifier the high-frequency instability is experienced at 2 MHz and eliminated by adding a 4 pF capacitor in series with a 20 $k\Omega$ resistor from the drain of NMOS, the second stage amplifier, to the ground.

A PTAT current is actually generated from a PTAT voltage source. Generating a PTAT voltage source uses the same equation as generating the bandgap reference, Equation (2). From Equation (2), the constant term is:

$$V_{PTAT}(T_r) = a_1 V_{BE1}(T_r) + a_2 V_{BE2}(T_r) \quad (14)$$

the first-order temperature dependency term is:

$$V_{1ST}(T) = \sum_{m=1}^{2} a_m \left[V_{BEm}(T_r) - V_{G1}(0) - (\eta - \theta_m)\frac{kT_r}{q}\right]\frac{T - T_r}{T_r} \quad (15)$$

and the second and higher-order temperature dependency terms is:

$$V_{REST}(T) = \sum_{m=1}^{2} a_m \sum_{n=2}^{\infty}\left[\alpha_n T_r^n - \frac{kT_r}{q}(\eta - \theta_m)\frac{(-1)^2}{2(2-1)}\right] * \left(\frac{T - T_r}{T_r}\right)^2 \quad (16)$$

If the current biasing both BJTs has same temperature dependency, then in order to eliminate the second and higher-order temperature dependency terms:

$$a_1 = -a_2 \tag{17}$$

This condition changes Equation (15):

$$V_{1ST}(T) = V_{PTAT}(T_r)\frac{T - T_r}{T_r} \tag{18}$$

which is a PTAT voltage. Exploring Equation (14):

$$V_{PTAT}(T_r) = \frac{kT_r}{q}\left[a_1 \ln \frac{I_{C1}(T_r)}{I_{S1}(T_r)} + a_2 \ln \frac{I_{C2}(T_r)}{I_{S2}(T_r)}\right] = \frac{akT_r}{q}\ln\left[\frac{I_{C1}(T_r)}{I_{S1}(T_r)}\frac{I_{S2}(T_r)}{I_{C2}(T_r)}\right] \tag{19}$$

where $a = a_1 = -a_2$.

If BJT_1 is biased with a current which is N times the current biasing BJT_2

$$I_{C1}(T_r) = N \cdot I_{C2}(T_r) \tag{20}$$

and the area of BJT_2 is M times the area of BJT_1

$$I_{S2}(T_r) = M \cdot I_{S1}(T_r) \tag{21}$$

then equation (19) becomes:

$$V_{PTAT}(T_r) = \frac{akT_r}{q}\ln(N \cdot M) \tag{22}$$

This shows that now the constant 'a' is not necessary to be set to a certain value. It shows also that the product of N and M have to be larger than one. If the PTAT voltage in equation (19) is across a resistor then the current flowing through the resistor is a PTAT current.

Figure 5 shows a common circuit topology to generate a PTAT current with a =1. The voltage across R_{PTAT} is a PTAT voltage. Therefore the current through it is a PTAT current, which biases Q_Z. This current is mirrored by PMOS pair M_Y and M_Z to bias Q_Y. Therefore the biasing current of Q_Z and Q_Y is of the same temperature behavior. BJT Q_Y in Figure 5 also functions as the reference BJT_1, as in Figure 3.

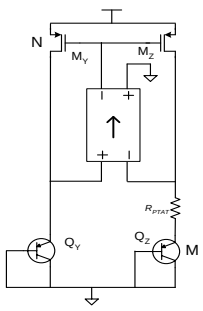

Figure 5. PTAT Current Source

For the frequency behavior analysis, it shows an instability at about 1.7 MHz which is then eliminated by putting a 4 pF capacitor in series with a 15 $k\Omega$ resistor between the gate of M_Y and M_Z and the ground.

5. Simulation Results

In this paper three simulation results are represented. They are the output of the PTAT current source circuit (Figure 6), the designed reference voltage (Figure 7) and the effect of the voltage source to the reference voltage (Figure 8).

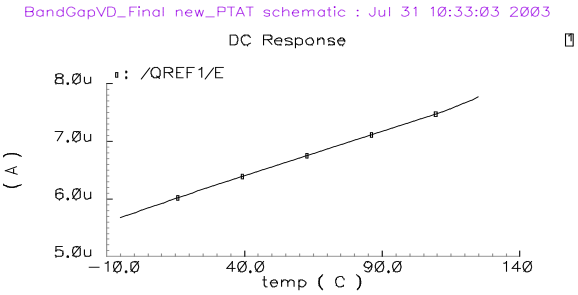

Figure 6. The Generated PTAT Current

The PTAT current source swings linearly from 5.76μA at 0°C to 7.66μA at 120°C or 15.83nA/K. Its output noise level is 0.58μV at 1kHz and 60°C.

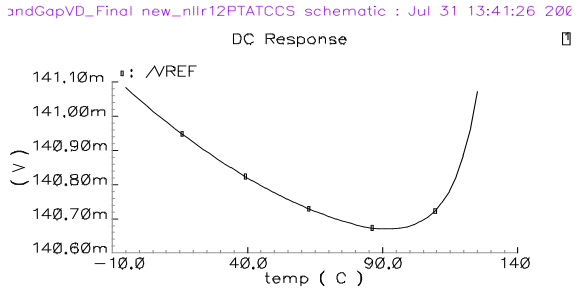

Figure 7. The Output of The Simulated Bandgap Reference.

The mean temperature dependency of the output voltage is about 22.5 ppm/K, in this condition the scaling factors a_1= 0.986 and a_2= 0.852. Its noise level is 1.823µV at 60°C and 1kHz..

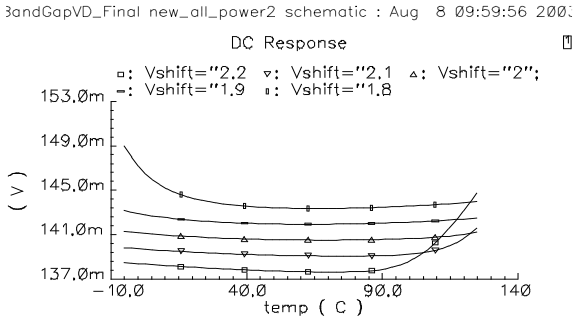

Figure 8. The Bandgap Output Voltage as The Function of The Temperature for Several Level of DC Voltage Supply

From Figure 9 it is shown that as the voltage supply is shifted further from the designed voltage level, the temperature dependency becomes higher.

6. Conclusion

In this research the design of the bandgap reference as well as a PTAT current source have been done and simulated. Due to the use of the substrate BJT, the scaling factor a_1= 1 can be achieved only by a scaling circuit. Therefore, the designed bandgap reference actually has still two scaling factors.

The designed bandgap reference circuit has an output voltage of 140mV and a temperature dependency of 22.5ppm/K. Its noise level about 57.6nV/√Hz. Its total current consumption is about 115μA from a 2V voltage-supply.

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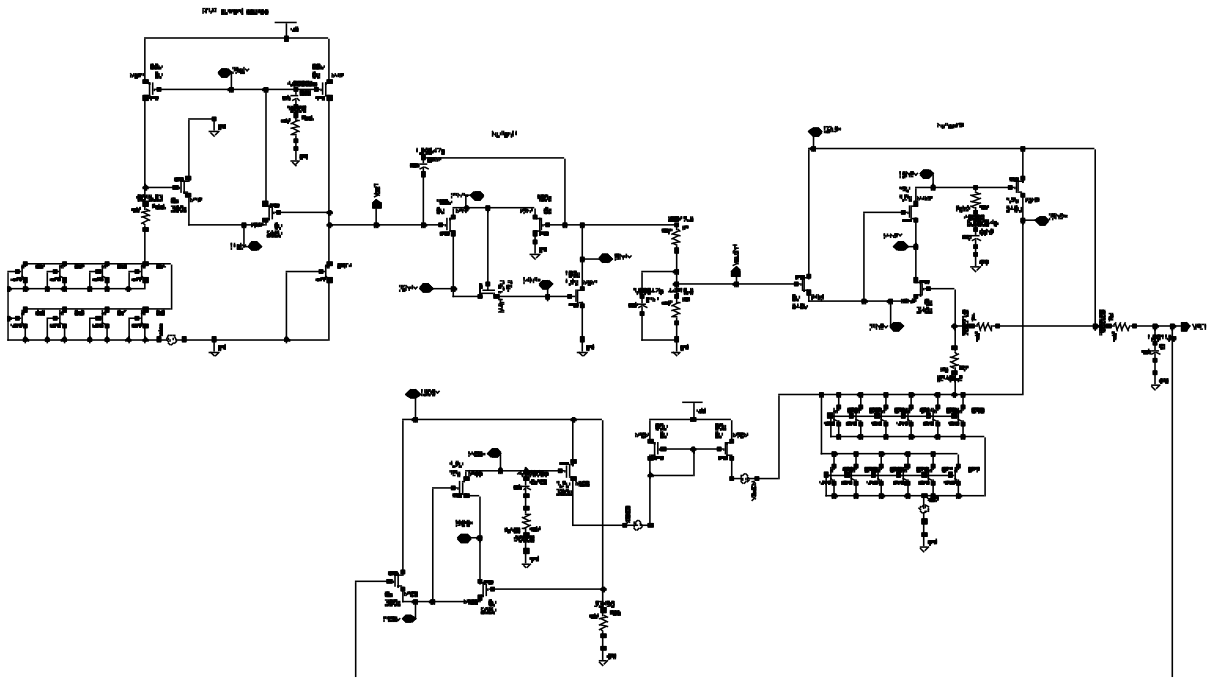
Attachment

The figure attached is the whole designed circuit. The supplying current sources are not shown.



The Schematic of The Designed Bandgap Reference Circuit